In The Claims

Please amend the claims as follows:

6. (Currently Amended) A semiconductor memory comprising:

one or a plurality of processor elements having arithmetic functions;

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair;

a plurality of first gate pairs;

a plurality of second gate pairs;

a plurality of first data line pairs of each to be connected with one of the bit line pairs selected by means of the first gate pairs and said data line pairs are dedicated for specific location column sub-block memory cells, on activation, and said plurality of processor elements are laidout to connect thereto; and

a plurality of second data line pairs to be connected with one of the first data line pairs by means of the second gate pairs to select specific row location of sub-block data consisting of crossbar crosspoint; wherein

the first data line pair and the second data line pair are arranged to intersect each other and said first gate pairs and second gate pairs are arranged along the side of sub-block sense amplifier.